

ABSTRACT

A semiconductor device including a vertical assembly of semiconductor chips interconnected on a substrate with one or more metal standoffs providing a fixed space between each supporting chip and a next successive vertically stacked chip is described. The device is fabricated by patterning islands of aluminum atop the passivation layer of each supporting chip simultaneously with processing to form bond pad caps. The fabrication process requires no additional cost, and has the advantage of providing standoffs for a plurality of chips by processing in wafer form, thereby avoiding additional assembly costs. Further, the standoffs provide improved thermal dissipation for the device and a uniform, stable bonding surface for wire bonding each of the chips to the substrate.